TRAINING & PLACEMENT CELL
COLLEGE OF TECHNOLOGY

CTE/TPC/ 4429
Dated: May 15, 2025

NOTICE

B. Tech & M. Tech
ECE, CS, EE and IT
(June 2026 Passing)

As per the communication received from **M/s NextlCron Technologies Pvt. Ltd. Bangalore** they are likely to visit our college on 2nd/3rd week of June 2025. They are looking for the B. Tech Third year & M. Tech students of ECE, CS, EE and IT. Third year students of these disciplines who are registered with the Training and Placement Cell of the College and have not been placed so far may confirm their interest in appearing for the campus interview by submitting their resume in the prescribed format in the T & P Cell between **12-01 pm and 3-5 pm on 19th May 2025.**

- **Eligibility Criteria:** 60% (X, XII and CGPA)
- **Selection Process:** Written Tests and interviews
- **Job Description Attached**

Students are advised to take timely necessary action accordingly.

15/05/2025

(B. K. Singh)
Officer I/C,
Training & Placement

Copy:
Notice Board NCT/PCT, Mandakni Bhawan & VS Bhawan
All concerned Students through E Mail
All Head's College of Technology for information and display on departmental notice boards
Director Placement & Counselling for kind information
Dean CT for kind information
In-charge College/ University Website for uploading

Job Description for Campus Interview at G. B. Pant Univ of Agri and Tech: Graduate Engineer and Trainee Engineer Positions

May 14, 2025

Company Overview: NextICron Technologies specializes in semiconductor IP design and services. Our expertise lies in developing high-quality semiconductor intellectual property solutions, tailored to meet the needs of our clients in the semiconductor industry. With our innovation-driven approach, we aim to deliver world-class products and services in the field of semiconductor design. Our India office is registered in Bangalore.

We are hiring Graduate Engineers and Trainee Engineers for multiple positions across various domains. Bachelor's and master's students from Electronics and Communication, Electrical, Computer and IT disciplines are welcome to participate. The selection process will be based on the right aptitude and attitude. CTC will be competitive to the industry standards.

Positions Available:

1. Layout [Trainee/Graduate/Associate] Engineer – salary band [5 Lakh – 14 Lakh]
    - Job Responsibilities:
        - Draw physical layouts of SRAM blocks and standard cells.
        - Perform DRC (Design Rule Check), LVS (Layout Versus Schematic), and Extraction.
        - Run IR/EM simulations to verify the layout integrity and reliability.
    - Skills Required:
        - Understanding of layout design and verification tools.
        - Basic knowledge of CMOS technology and design principles.
2. Design/Automation [Trainee/Graduate/Associate] Engineer -salary band [5.5 Lakh - 18 Lakh]
    - Job Responsibilities:
        - Create and simulate circuit schematics for various components and blocks.
        - Run design margin and characterization simulations.
        - Analyze simulation results and optimize designs.
        - Write software automation scripts for design margin checks, characterization, and simulation.
        - Develop and maintain automated workflows to streamline the design process.
    - Skills Required:
        - Knowledge of analog and digital circuit design.
        - Familiarity with simulation tools and circuit analysis techniques.

- Proficiency in programming languages such as Python, Perl, or Shell scripting.
- Understanding of circuit design and simulation processes.

Eligibility:

- Open to 3rd year/Final year bachelor's and final year Master's students from Electronics and Communication, Electrical, Computer, and IT Engineering backgrounds. Minimum GPA 6.0
- Selection based on aptitude (logical reasoning, problem-solving) and attitude (learning mindset, willingness to collaborate).

Selection Process:

1. Written Test:
   - For Electronics and Communication Engineering (ECE) students:
     - Questions related to basic digital electronics, CMOS processing steps, basic gates layout, stick diagram, schematic and truth tables, SRAM operation, and circuits.
   - For students from other branches (Electrical, Computer, and IT Engineering):
     - Selection will be based on GPA, programming knowledge, and an aptitude test.
     - The programming test will assess the candidate's coding and problem-solving abilities in languages such as C, C++, Python, or Java.
   - **No written test for previous short listed and summer Interns.**
2. Interview:
   - Technical interview to assess the candidate's domain knowledge.
   - Evaluation of aptitude, problem-solving skills, and approach to real-world engineering challenges.

If you have the right aptitude, a passion for technology, and the drive to grow in an exciting engineering environment, we would love to meet you!